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### REMARKS

Claims 2, 6-8, 25-36, 47, 49-51, 53-58, and 60-62 are pending in the present application. Claims 58 and 60-62 depend from elected claims but should be withdrawn from consideration as be directed to a non-elected species. The present application, as amended, includes seven independent claims - 2, 6-8, 49, 50, and 57. Each of the presently pending claims includes recitations covering the manner in which the decoupling capacitors of the claimed device are accommodated within the claimed structure.

Specifically, **independent claims 2 and 7**, the recitations of which can be illustrated conveniently with reference to Figs. 3 and 6 of the present application, recite a decoupling capacitor 60 and a multiple die semiconductor assembly comprising an intermediate substrate 40 positioned between first and second semiconductor dies 20, 30. The thickness dimension of the decoupling capacitor 60 is accommodated in a space defined by the thickness dimension of the first semiconductor die 20. These claims have been amended to clarify the nature of the "thickness" dimensions. Specifically, as is clearly illustrated in the original figures, the claim recites that the "respective thickness dimensions" of the decoupling capacitor and the first semiconductor die "are oriented perpendicular to said first surface of said intermediate substrate."

**Independent claims 6, 8 and 57**, the recitations of which can be illustrated conveniently with reference to Figs. 1 and 7 of the present application, recite a multiple die semiconductor assembly comprising a decoupling capacitor 60 and an intermediate substrate 40 positioned between first and second semiconductor dies 20, 30. A topographic contact 12 extends between the first surface 42 of the intermediate substrate 40 and the first active surface 22 of the first semiconductor die 20. The topographic contact is defined in the specification as comprising "any conductive contact that extends between and defines a spacing between an active surface of a substrate or die and an active surface of another substrate or die (see page 11, lines 22-24)." These three independent claims also recite that the thickness dimension of the decoupling capacitor 60 is accommodated in a space defined by the thickness dimension of the topographic contact extending between the first surface 42 of the intermediate substrate 40 and the first active surface 22 of the first semiconductor die 20. The respective thickness dimensions of the

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decoupling capacitor and the topographic contact are recited in the claims as being "oriented perpendicular to said first surface of said intermediate substrate."

**Independent claim 49**, the recitations of which can be illustrated conveniently with reference to Fig. 4 of the present application, recites a multiple die semiconductor assembly comprising an intermediate substrate 40 positioned between first and second semiconductor dies 20, 30. A first surface 82 of an additional substrate 80 faces the second active surface 32 of the second semiconductor die 30. A decoupling capacitor 60 is mounted to the first surface 92 of a third substrate 90, which faces the second surface 84 of the additional substrate 80. The thickness dimension of the decoupling capacitor 60 is accommodated in a space defined by the thickness dimension of the topographic contact 12 extending from the second surface 84 of the additional substrate 80 to a first surface 92 of the third substrate 90. Again, the respective thickness dimensions are recited in the claims as being "oriented perpendicular to" the second surface 84 of the additional substrate 80.

**Independent claim 50**, the recitations of which can be illustrated conveniently with reference to Fig. 5 of the present application, recites a multiple die semiconductor assembly comprising an intermediate substrate 40 positioned between first and second semiconductor dies 20, 30. An additional substrate 80 is positioned such that its first surface 82 faces the second active surface 32 of the second semiconductor die 30. A third substrate 90 is positioned such that the first surface 42 of the intermediate substrate 40 faces the second surface 94 of the third substrate 90. A decoupling capacitor 60 is mounted to the second surface 94 of the third substrate 90. As is illustrated in Fig. 5, the thickness dimension of the decoupling capacitor 60 is accommodated in a space defined by the thickness dimension of the topographic contact 12 extending from the second surface 94 of the third substrate 90 to the first surface 42 of the intermediate substrate 40. The respective thickness dimensions are recited in the claims as being "oriented perpendicular to" the first surface 42 of the intermediate substrate 40.

As is further illustrated in Fig. 5, **claim 51, which depends from claim 50**, further recites that the thickness dimension of the decoupling capacitor 60 and the thickness dimension of the first semiconductor die 20 are both accommodated in said space defined by the thickness dimension of the topographic contact 12.

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Accordingly, each of the above-described groups of claims define structure that represents advances in semiconductor packaging and, as pointed out in the present specification, structure that represents “an improved scheme for increasing semiconductor die density” (see page 1 of the present application, lines 12-13). In contrast, the examiner has asserted that “with respect to the rearrangements of the [decoupling] capacitors, absent some teaching of criticality it would have been an obvious matter of design choice to place the capacitor anywhere in the package” (see para. 16 of the 11/3/2004 Office Action). However, applicants assert that because the specific arrangements recited in the presently pending claims are particularly directed at increasing semiconductor die density, they rise beyond a mere matter of obvious design choice. Indeed, this assertion is buttressed by the fact that none of the cited references, taken alone or in combination, teach the arrangements recited in claims 2, 6-8, 49, 50, 51 and 57. As the Examiner notes correctly in the latest Office Action, the mere fact that one skilled in the art could rearrange the parts of a reference device to meet the terms of the presently pending claims is not by itself sufficient to support a finding of obviousness.

The Examiner has expressed reservations that the thicknesses recited in the claims can be understood to mean a thickness dimension defined anywhere in the claimed assembly because the space in a particular thickness dimension can be defined by a plane that extends in any direction, crossing anywhere in the assembly. To address this point, the applicants have amended each of the presently pending independent claims to recite the respective thickness dimensions in a manner which is consistent with the thickness dimensions *a*, *b* illustrated in detail in Fig. 1 of the application, as filed.

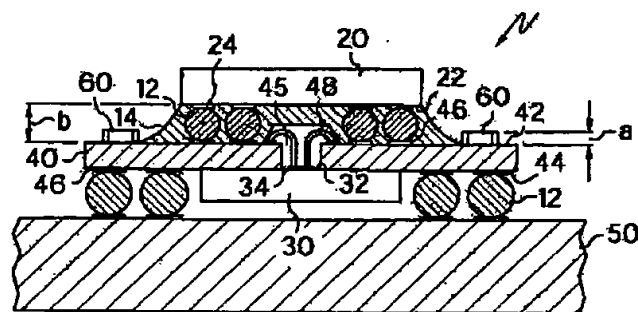


FIG. 1

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Applicants again respectfully submit that all one of ordinary skill could reasonably be expected to glean from the combination of the cited references is that it might be beneficial to provide a decoupling capacitor in some part of the prior art structure.\* None of the references provide any guidance suggesting that the thickness dimension of the decoupling capacitor, or the decoupling capacitor and the associated die, be accommodated in the particular spaces and locations defined in the presently pending claims.

### CONCLUSION

Applicants respectfully submit that the present application is in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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\* This statement is made for the purposes of illustration only and should not be taken as an admission by applicants that it would have been obvious to provide a decoupling capacitor in some part of the structure of Venkateshwaran et al.